



FIG. 4

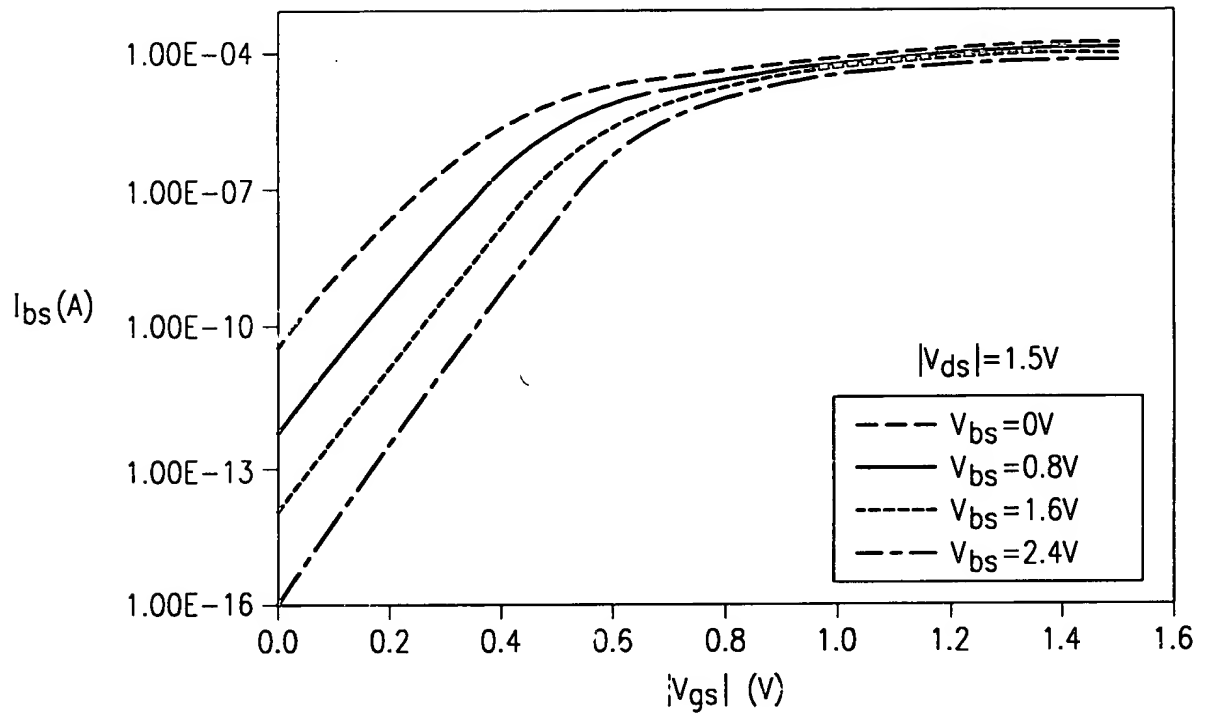
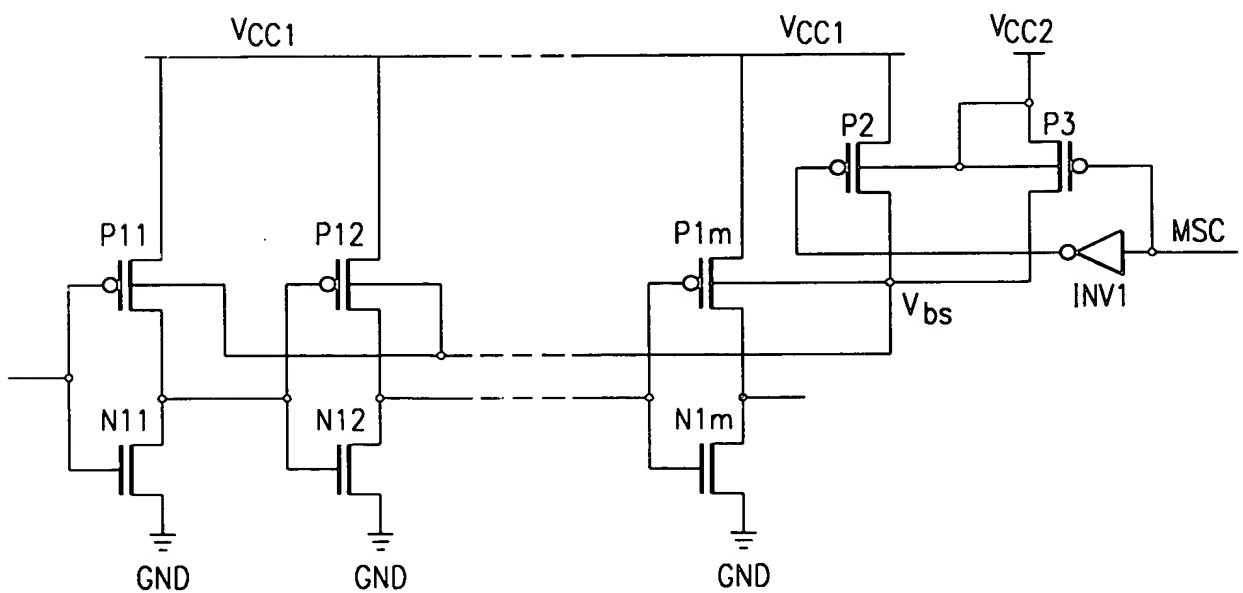


FIG. 6



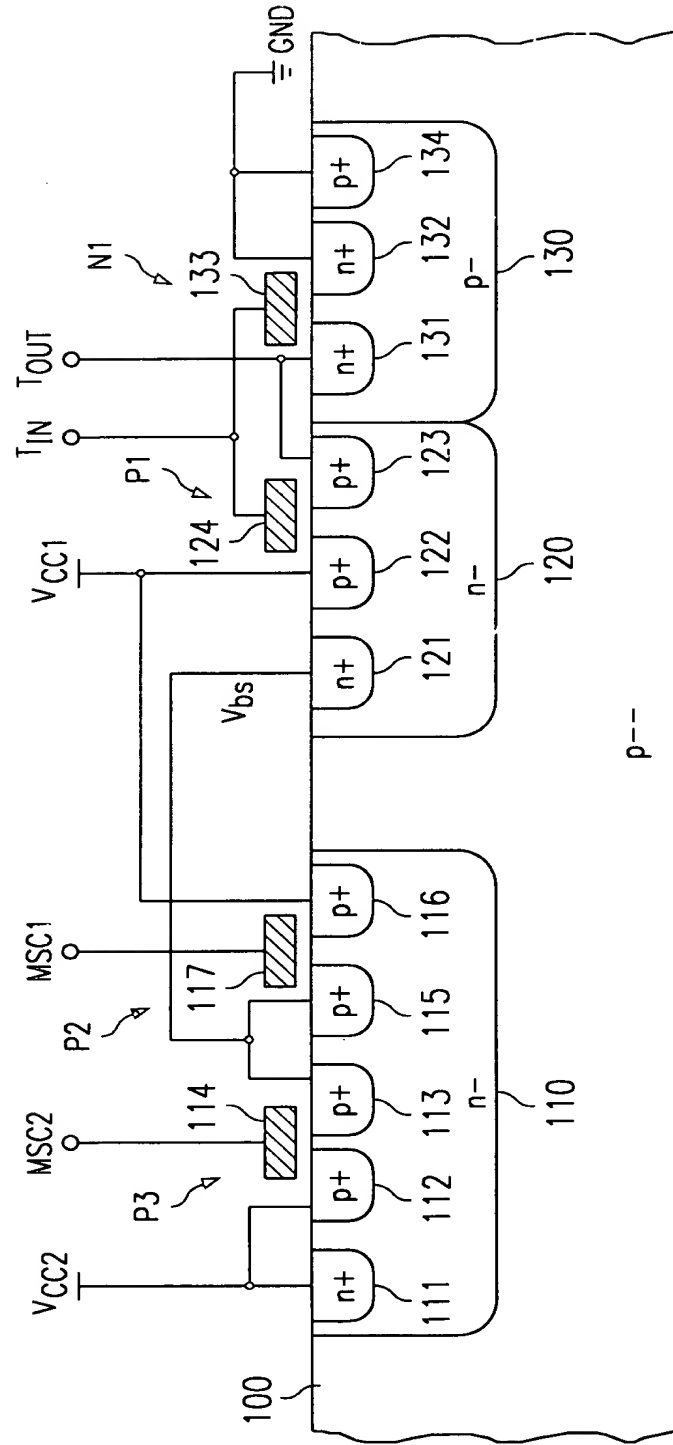
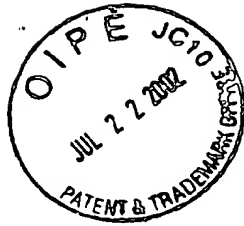


FIG. 5

FIG. 7

The diagram shows a differential amplifier circuit with two main branches. The left branch consists of a PMOS transistor P1 and an NMOS transistor N1. The input T_{IN} is connected to the gate of P1. The source of P1 is connected to V_{CC4} , and its drain is connected to the output T_{OUT} . The gate of N1 is connected to T_{OUT} , its source is connected to ground, and its drain is connected to the gate of N2. The right branch consists of a PMOS transistor P3 and an NMOS transistor N2. The gate of P3 is connected to V_{CC3} , its source is connected to V_{CC2} , and its drain is connected to the output $MSC3$. The gate of N2 is connected to the drain of N1, its source is connected to V_{SS1} , and its drain is connected to $MSC3$. There are also two inverters, INV1 and INV2. INV1's input is connected to the source of P3, and its output is connected to the source of P2. INV2's input is connected to the source of N2, and its output is connected to the source of N3. The gates of P2 and N3 are connected to V_{CC3} and ground respectively.

The diagram shows a CMOS inverter circuit. The input signal S_{IN} is connected to the gate of an NMOS transistor (N10). The output of the inverter, S_{OUT} , is connected to the gates of both the NMOS transistor (N10) and a PMOS transistor (P10). The PMOS transistor (P10) has its source connected to V_{CC} and its drain connected to the output node S_{OUT} . The NMOS transistor (N10) has its source connected to ground (GND) and its drain connected to the output node S_{OUT} . A threshold control voltage supply circuit (10) is connected to the gates of both transistors. The supply circuit provides a PMOS threshold voltage V_{bsp} to the gate of P10 and an NMOS threshold voltage V_{bsn} to the gate of N10.